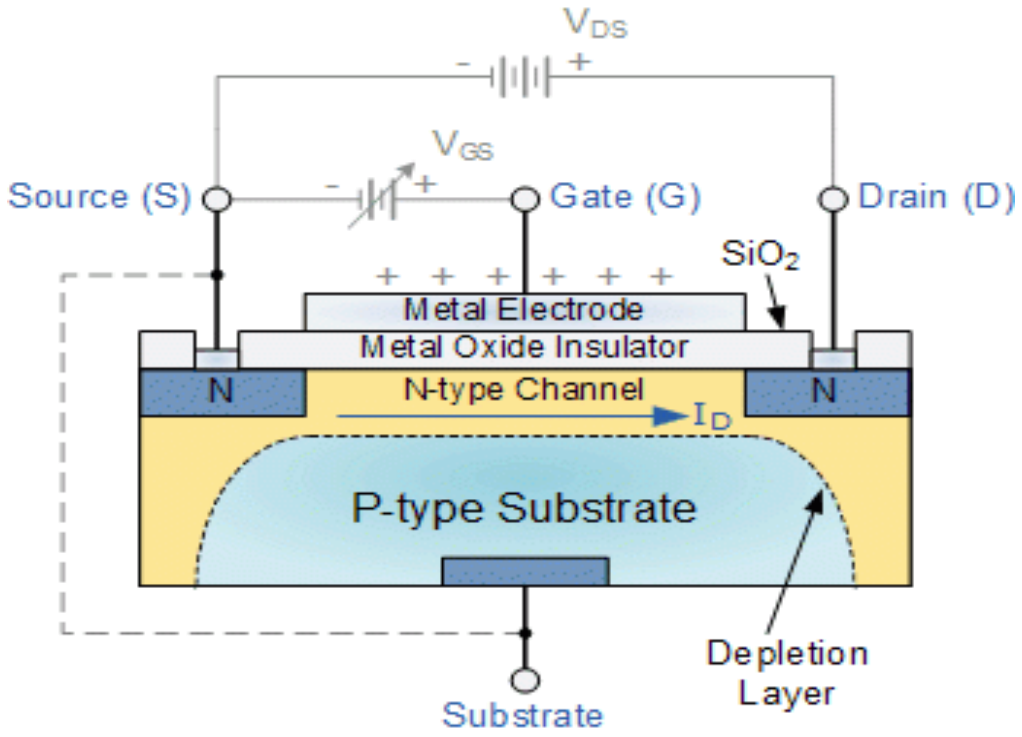
Identifying the best two-dimensional channel material for the reinstatement of complexity scaling in floating gate FETs



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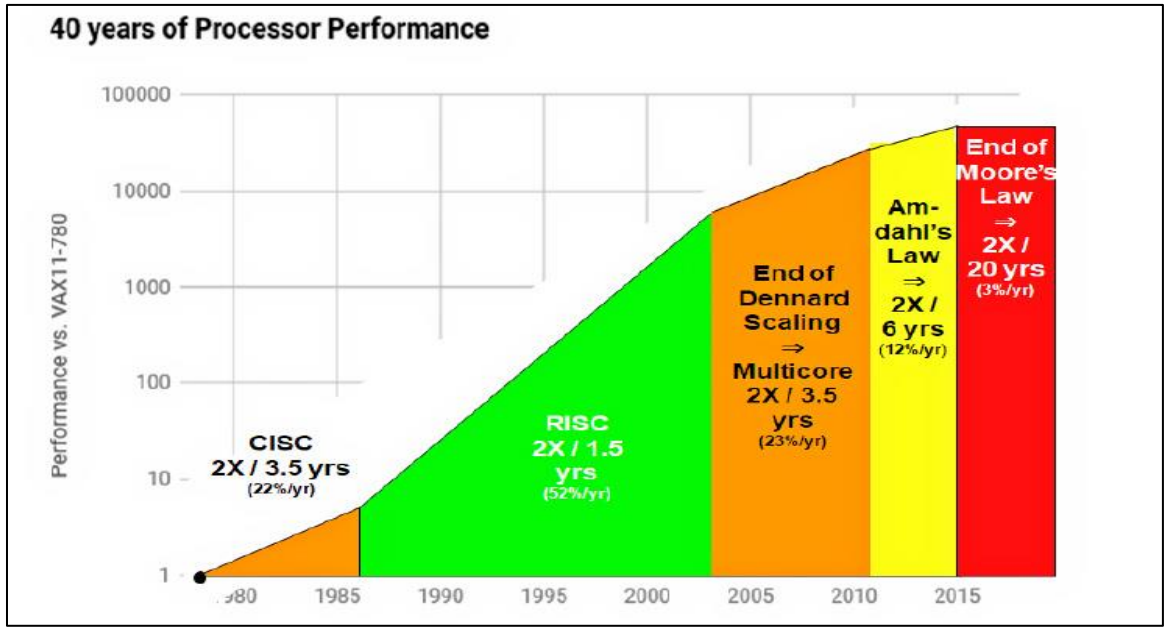
https://www.electronics-tutorials.ws/transistor/tran_6.html

The death of Moore's Law?

Gordon Moore adjusted his 1965 law (Moore's Law) and established that the number of transistors on microprocessors was going to double every two years instead of every year.



Since 2005, transistor scaling has been limited by energy, size and complexity scaling. In recent years, some scientists have even associated these scaling problems with an upcoming expiration of Moore's Law.

https://www.amazon.es/Intel-i5-3210M-Processor-Cache-2-5GHz/dp/B009AG8BME

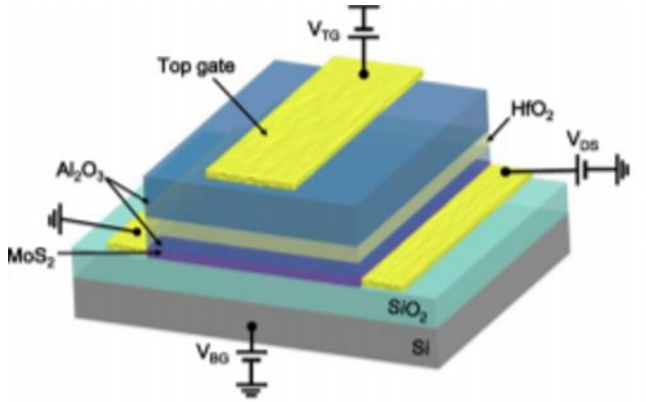
http://dis.um.es/~lopezquesada/documentos/IES_1415/LMSGI/curso/css/css14/html/mooregordon.html

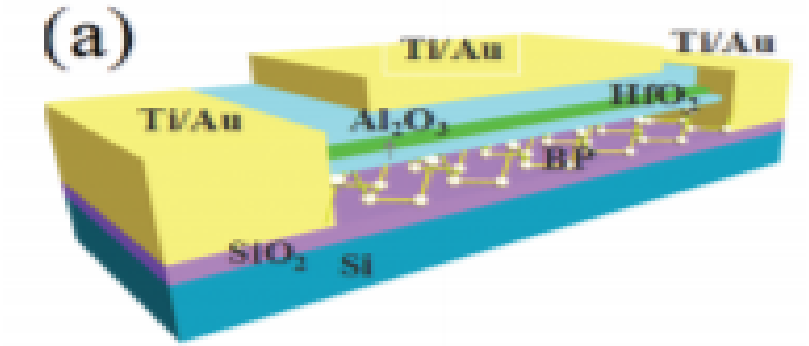
https://www.microcontrollertips.com/beyond-moores-law-new-solutions-beating-data-growth-curve/

Objectives

In order to reinstate the complexity scaling:

- ❑Floating-gate FETs are going to be studied in more detail through literature search.
- ❑An $Al_2O_3/HfO_2/Al_2O_3$ (AHA) gate stack structure will be explored to implement non-volatile memory (NVM).
- ❑ Various 2D materials will be explored to identify the best material for floating-gate FETs





DOI: 10.1039/c5nr08065g

DOI:10.1021/nn5059419

Previous challenges

Challenges:

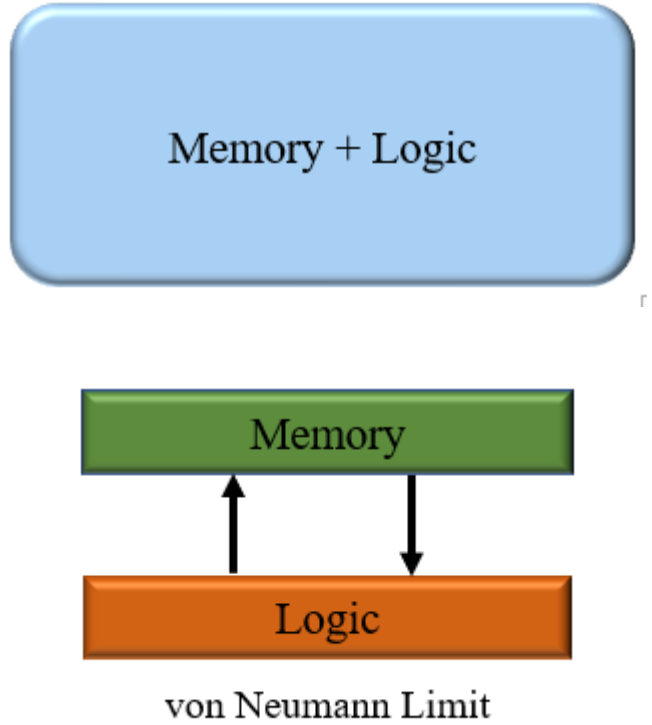
On the nanoscale, electron-based devices can depart drastically from the ideal behavior.

- Increased gate leakage currents and higher off state power consumption.

Von Neumann bottleneck affects the transfer rate between memory and logic units.

Enhance the performance of FG-FETs by conjoining few-layer 2D materials (graphene, black phosphorus, WSe_2, MoS_2) with the AHA gate stack.

More updated literature to be reviewed.



von Neumann Limit

Floating-gate FETs (FG-FET) and reinstatement of complexity scaling

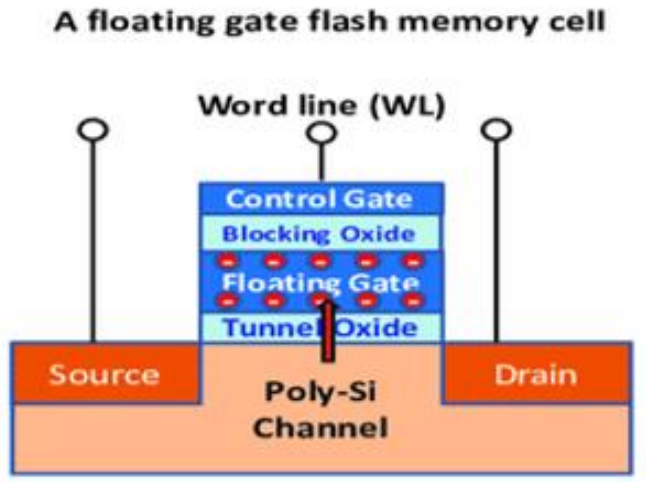
What is a floating-gate FET (FG-FET)?	Field effect transistor that has an additional gate between two insulators which can store electrons when the power goes out.
Non-volatile memory (NVM)	A type of memory that can retain stored data even after the power is turned off.
Complexity scaling	Floating gates allow in-memory processing potentially helping in reinstate complexity scaling of transistors.

FLASH Memory Operation and Floating-gate FETs

If we compare a flash memory cell to a transistor, the flash memory cell has an additional gate known as the floating gate.

There's no direct electrical contact available to the floating gate and it's surrounded by oxide material.

To warrant a large change in threshold voltage with programming, the tunnel oxide must be thinner than the blocking oxide.



https://www.exportersindia.com/aman-creative-graphic-designer/sd-memory-cards-3776683.htm

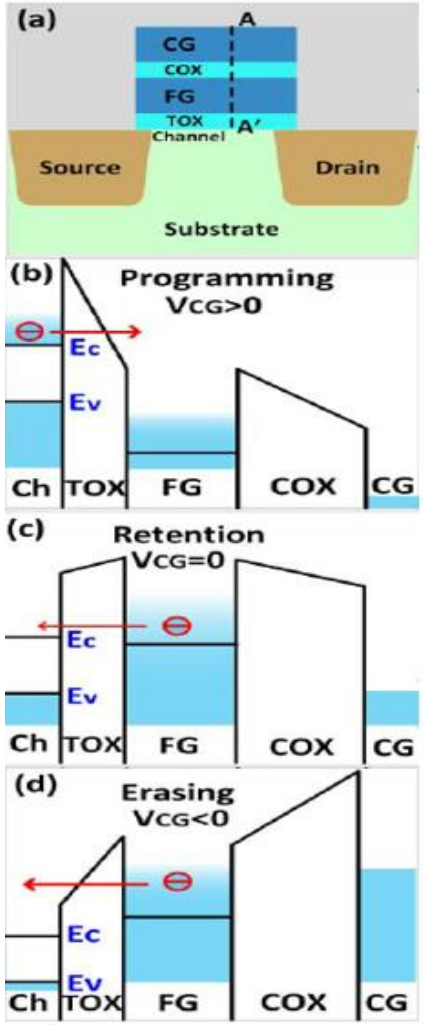
https://www.researchgate.net/figure/a-A-floating-gate-FG-NAND-Flash-memory-cell-which-stores-charge-in-the-FG-Metal_fig1_327007460

A deeper look into the physics of floating-gate FETs (FG-FET)

Whenever we are programming a FLASH memory cell, we apply a high gate voltage so that a high program current can be reached.

If we intend to retain the charge in the floating gate, we must not apply a gate voltage.

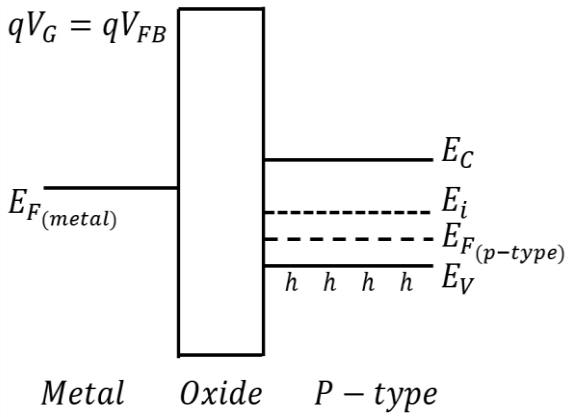
During the erase operation, a large negative voltage is required to repel electrons from the floating gate.

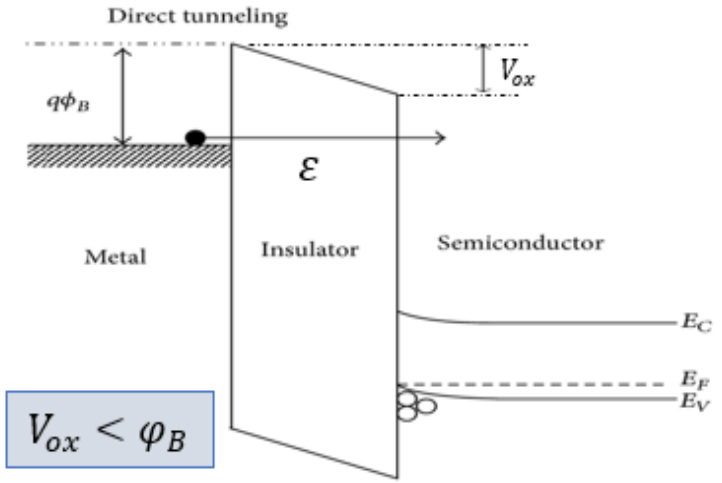


https://www.researchgate.net/figure/a-Cross-section-of-a-typical-FG-transistor-Band-diagrams-and-electron-transport_fig1_278116086

A deeper look into the physics of floating-gate FETs (FG-FET)

In a **flat band,** there is no potential difference between the semiconductor and the metal gate.





$V_{ox} < \varphi_B$

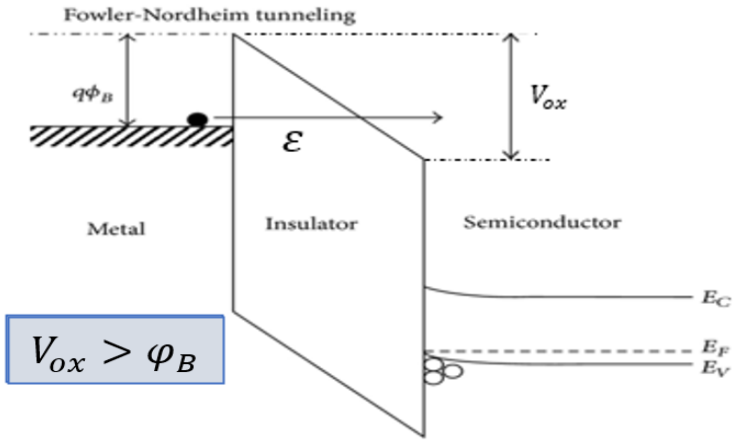
In **direct tunneling**, the electrons tunnel through a trapezoidal-shaped barrier.

Equation:

$$J_{DT} = \frac{k_1 \varepsilon^2}{\left(\sqrt{\varphi_B} - \sqrt{\varphi_B - V_{ox}}\right)^2} exp\left\{\frac{-k_2\left[\varphi_B^{3/2} - (\varphi_B - V_{ox})^{3/2}\right]}{\varepsilon}\right\}$$

The **Fowler-Nordheim (F-N) tunneling** occurs at a higher gate voltage than the direct tunneling. The electrons tunnel through a triangle-shaped barrier.

Equation: $J_{FN} = \frac{k_1 \varepsilon^2}{\varphi_B} exp\left[\frac{-k_2\left(\varphi_B^{3/2}\right)}{\varepsilon}\right]$



$V_{ox} > \varphi_B$

https://www.hindawi.com/journals/amse/2014/578168/fig8/

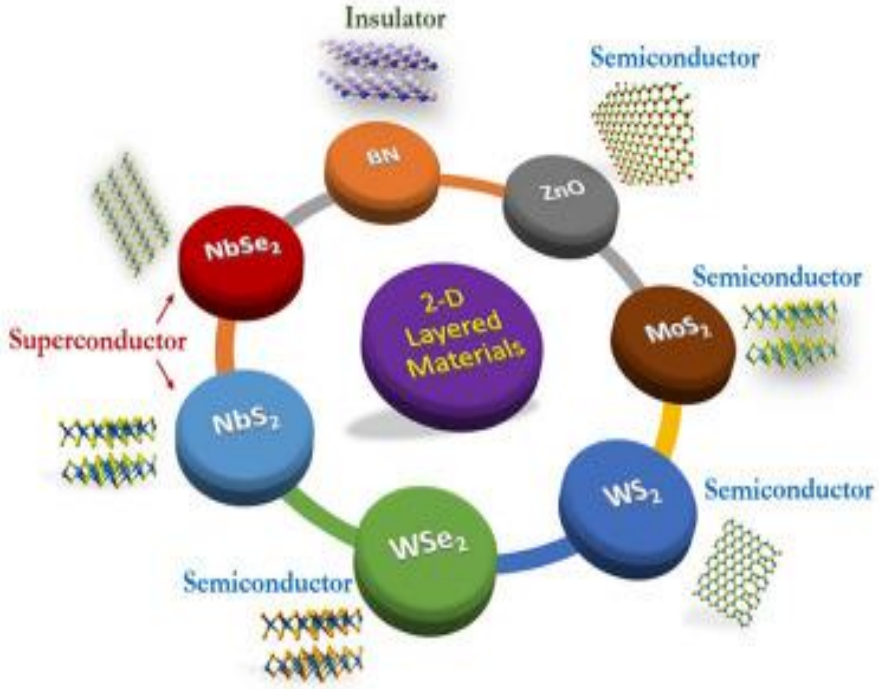
https://commons.wikimedia.org/wiki/File:MOS_flat_band.png

https://www.researchgate.net/figure/Schematic-energy-band-diagram-of-Fowler-Nordheim-tunneling-in_fig17_270628576

Applications of 2D materials in floating-gate FETs

The FET community has shifted its interest to:

- 2D materials with sizable (>0.3 eV) bandgaps
- low off-state currents
- high on-state currents



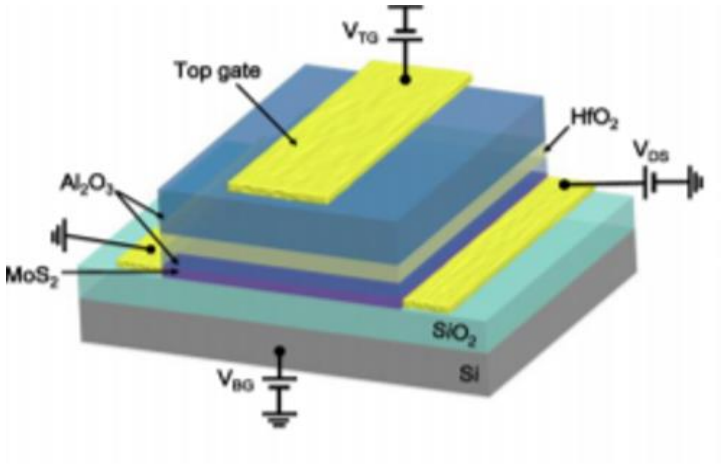
Transition metal dichalcogenides (TMDs) have emerged as the most promising candidate for novel semiconductor device applications.

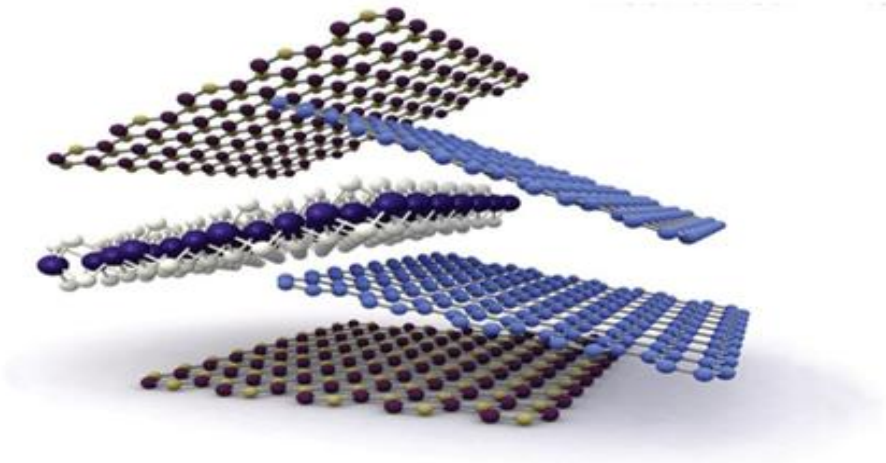
- wide and controllable band gap.

https://tsapps.nist.gov/publication/get_pdf.cfm?pub_id=926951

https://www.sciencedirect.com/science/article/abs/pii/S1748013215000961

$Al_2O_3/HfO_2/Al_2O_3$ (AHA) and 2D materials





$Al_2O_3/HfO_2/Al_2O_3$ gate stack structure:

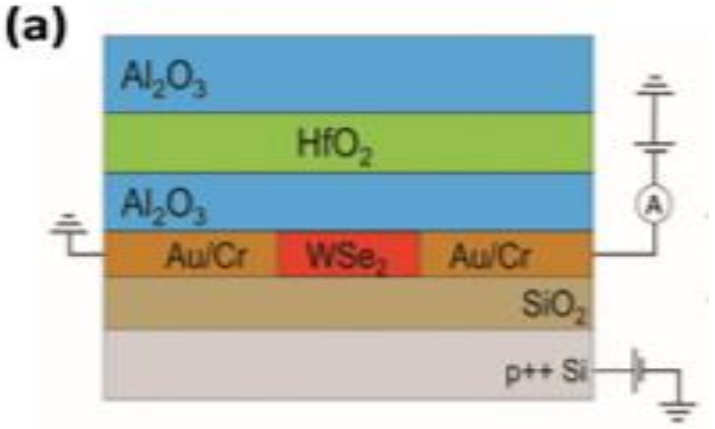
- Shallow hole potential well (ϕw-h = 0.15 ev)
- Deep electron potential well (ϕw-e = 1.15 ev)
- Transparent and flexible features
- Reduces crosstalk between different cells
- Good scalability

2D materials without dangling bonds possess:

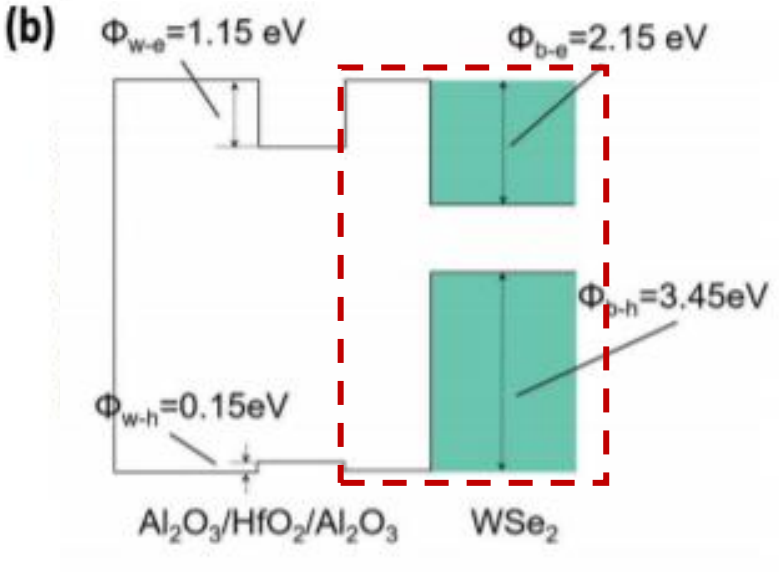
- Excellent electronic properties
- Perfect interfaces (free of charge traps)
- High carrier mobility and large ON/OFF current ratio
- Transparency and flexibility
- Large band gap

DOI: 10.1039/c5nr08065g https://sci-hub.tw/https://doi.org/10.1016/j.tsf.2008.08.047 https://science.sciencemag.org/content/353/6298/aac9439

Improvements in the charge-trap memory device



The WSe_2 floating-gate phototransistor exhibits a large memory window and hold time.



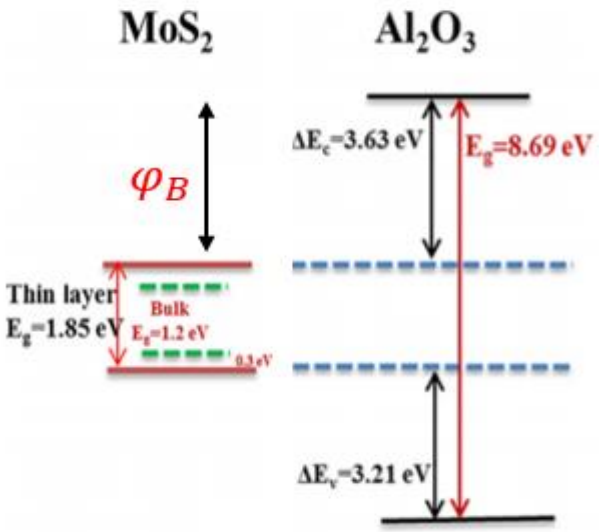
Combining WSe_2 with the $Al_2O_3/HfO_2/Al_2O_3$ stack structure in a non-volatile FLASH memory allows a high writing speed without over-erase phenomena.

10.1002/smll.201604128

Valence and conduction energy bands

Band Offset → Energy difference between bands (either conduction and valence band) of different materials. These values define the confinement potentials for carriers.

- **Valence Band Offset (VBO)**
- **Conduction Band Offset (CBO)**



Direct Tunneling

$$J_{DT} = \frac{k_1 \varepsilon^2}{\left(\sqrt{\varphi_B} - \sqrt{\varphi_B - V_{ox}}\right)^2} exp\left\{\frac{-k_2\left[\varphi_B^{3/2} - (\varphi_B - V_{ox})^{3/2}\right]}{\varepsilon}\right\}$$

FN Tunneling

$$J_{FN} = \frac{k_1 \varepsilon^2}{\varphi_B} exp\left[\frac{-k_2\left(\varphi_B^{3/2}\right)}{\varepsilon}\right]$$

Band offsets of 2D channel materials in floating-gate FETs

2D Material	Conduction Band Offset (CBO) with Al_2O_3	Valence Band Offset (VBO) with Al_2O_3	|CBO - VBO|
$MoSe_2$	1.92 eV	4.59 eV	2.67 eV
MoS_2	3.63 eV	3.21 eV	0.42 eV
Graphene	2.43 eV	1.58 eV	0.85 eV
WS_2	3.56 eV	2.79 eV	0.77 eV
WSe_2	2.15 eV	3.45 eV	1.30 eV

10.1016/j.apsusc.2019.144521 10.1063/1.4963289

https://tsapps.nist.gov/publication/get_pdf.cfm?pub_id=926951

https://aip.scitation.org/doi/am-pdf/10.1063/1.4963289#:~:text=Thin%20layer%20MoS2%2FAl2O3%20and,3.63%20eV%20and%201.27%20eV.

Conclusions and future recommendations

The VBO and CBO values of **MoS_2** are symmetric; therefore, it can be used **as a channel material** for the AHA gate stack structure in floating-gate FETs.

The **low leakage current** and **high breakdown field** that 3,4,9,10-perylene-tetracarboxylic dianhydride (PTCDA) offers can substitute the properties of Al_2O_3 as a tunneling oxide material.

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